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10EC56

# Fifth Semester B.E. Degree Examination, June/July 2015
## Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

### PART – A

1 a. Discuss the nMOS enhancement mode transistor for different conditions of vds. **(06 Marks)**

b. Elaborate the concept of P-well falorication with neat sketches. **(10 Marks)**

c. Compare CMOS and bipolar technologies. **(04 Marks)**

2 a. Obtain the transfer characteristics of a CMOS inverter and mark all the regions. Showing the status of PMOS and NMOS transistors. **(10 Marks)**

b. Illustrate the schematic and stick diagram for the expression $Y = \overline{A(B+C)}$. **(10 Marks)**

3 a. Discuss in detail the $\lambda$ - based design for CMOS. **(10 Marks)**

b. Realize a 3-input NAND gate for clocked CMOS logic and also for CMOS domino logic. **(06 Marks)**

c. Discuss the working of pseudo nMOS logic with suitable example. **(04 Marks)**

4 a. Describe the delay unit $\tau$ in terms of sheet resistance and area capacitance for the CMOS inverter pain shown, calculate the total delay. **(08 Marks)**


Fig. Q4(a)

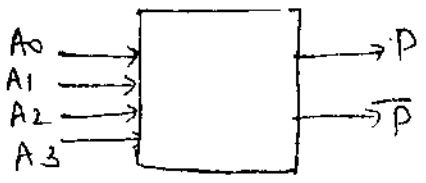
b. Explain in brief the wiring capacitances. **(06 Marks)**

c. Narrate the steps involved in calculate the sheet resistance of :
i) Transistor channel ii) nMOS inverter iii) CMOS inverter. **(06 Marks)**

### PART – B

5 a. What are the scaling factors for the following device parameters :
i) Gate capacitance $c_g$ ii) max-operating frequency $f_0$ iii) current density iv) power dissipation per gate $p_g$ v) power speed product PT. **(10 Marks)**

b. Design a parity generator with the following specifications and draw the stick diagram of one basic cell. **(10 Marks)**




$$P = \begin{cases} 1, & \text{even numbers of 1's} \\ 0, & \text{odd numbers of 1's} \end{cases}$$

Fig. Q5(b)

6 a. Draw the basic form of a two-phase clock generator and explain in detail. **(08 Marks)**
b. Discuss the architectural issues to be followed in the design of a VLSI subsystem. **(06 Marks)**
c. Explain the precharge bus approach used in system design. **(06 Marks)**

7 a. Explain the three transistor dynamic RAM cell. **(10 Marks)**
b. Discuss the Bangh-Wooley method used for two's complement multiplication. **(10 Marks)**

8 a. Narrate the meaning of "Real Estate" in VLSI design. **(05 Marks)**
b. Explain testing and testability in detail. **(10 Marks)**
c. Write a short note on scan design techniques. **(05 Marks)**

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